



EXAMEN SESSION PRINCIPALE SEMESTRE 1

A.U:	2021/2022	Cycle:	Ingénieurs
Module :	Digital circuits	Level :	1st Year
Time	09H - 11H	Field	Tronc commun
Date	13/01/2022	Durée :	2h
Documents:	Not Authorized	N° pages:	2

Exercise	1	2	3
C.L.Os Assesment	K1, S2, V4	K1, S2	S2 ; V4

Exercise 1 (6pts)

Consider Figure 1 below.

1. Give the logical expression F realized by this figure?
2. Simplify the expression F (Use De Morgan's theorem or Karnaugh's table).
3. Establish a simplified scheme allowing the realization of the expression F

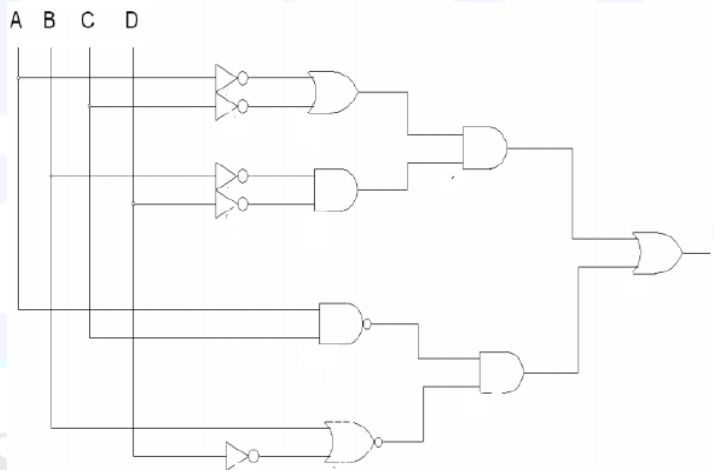


Figure.1

Exercise 2 (6pts)

1- What is the output logic equation F of the multiplexer represented on scheme 2

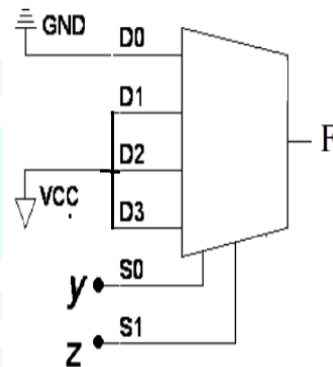


Figure 2

2- Using a multiplexer with 2 control inputs, perform the following function F:

$$F = \overline{A} \overline{B} \overline{C} + \overline{A} B C + A B \overline{C}$$

2- using only the NOR gate, determine the logic circuit relating to the expression X

$$X = \overline{A} B + A \overline{B}$$

Exercise 3 (8pts)

In figure 3 below, a transcoder with 4 inputs are called A, B, C, D and the 7 outputs are called a, b, c, d, e, f, g. When displaying the number 6 and from the number 9 segments **a** and **d** are lit.

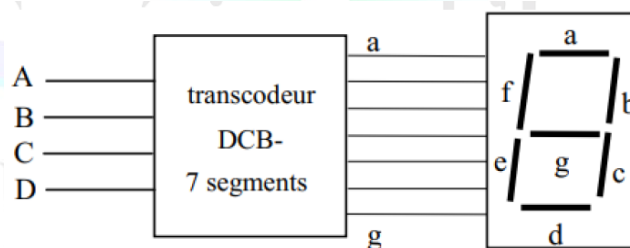


Figure 3

1°) Give the logic equations, depending on the inputs (A B C D), of the logic functions Fa and Fd are equal to 1 if the segments A and D are on.

2°) Using the Karnaugh tables simplify the previous equations

3°) Establish a diagram for the Fa function with a minimum of NAND and NOR gates

4°) Establish a diagram for the Fd function using a multiplexer with 3 control inputs