Course Title:	**Processor design methodology**
Course Code:	CSE311
Program:	Master Degree In Computer Engineering
Department:	Computer Engineering
Course coordinator:	Dr. Oussama boufares
Institution:	Private Higher School of Engineers of Gafsa (ESIP)

A. Course Identification

1. Credit hours: 3 (2-1-0)

2. Course type

a. College ☐ Department ■ Others ☐

b. Fundamental ■ Transversal ☐ Optional ☐

3. Level/year at which this course is offered: 2.1/3

4. Pre-requisites for this course : Digital circuits(CSE122), Architecture & micro processors(CSE242), CSE231

1. Mode of Instruction (mark all that apply)

No	Mode of Instruction	Contact Hours	Self-study	Total workload
1	**Traditional classroom**	…..	35	80
2	**Blended**	45		
3	**E-learning**	.....		
4	**Distance learning**	.....		
5	**Other ()**	.....		

2. Contact Hours (based on academic semester)

No	Activity	Contact Hours
1	**Lecture**	30
2	**Laboratory/Studio**	-
3	**Tutorial**	15
4	**Others** (specify)	-
	Total	45

B. Course Objectives and Learning Outcomes

Course Description

This course introduces the design and implementation of processors, focusing on the MIPS R3000 architecture. Students will explore instruction set architecture (ISA), arithmetic operations, single-cycle and multi-cycle processor design, and pipelining concepts. Through theoretical learning and practical labs, they will analyze processor performance and understand modern CPU design methodologies.

Course Main Objective

This course aims to:

- ✓ Understand the fundamentals of computer organization and processor design.
- ✓ Analyze instruction set architecture and its impact on performance.
- ✓ Implement single-cycle and multi-cycle processor designs.
- ✓ Explore pipeline concepts and hazard handling techniques.
- ✓ Develop and test processor simulations using MIPS simulators.

1. Course Learning Outcomes

CLOs		Aligned PLOs
	Knowledge and Understanding	
1.1	Explain the fundamental principles of MIPS processor architecture, including instruction set design and arithmetic operations.	PLO.K1
	Skills	
2.1	Design and implement single-cycle and multi-cycle processor architectures using simulation tools.	PLO.S.2
3.1	Analyze the impact of pipelining on CPU performance and solve pipeline hazards.	PLO S5

C. Course Content

No	List of Topics	Contact Hours
1	Chapter 1: Organization and Design of Computers 1. Overview of computer architecture and organization. 2. Components of a processor (CPU, memory, I/O). 3. Performance evaluation and metrics (CPI, MIPS, FLOPS). 4. RISC vs. CISC architectures.	6
2	Chapter 2: The Architecture of the Instruction Set 1. Introduction to Instruction Set Architectures (ISAs). 2. MIPS R3000 instruction set (registers, addressing modes, instruction types). 3. Memory organization and addressing (stack, heap, memory hierarchy). 4. Assembly language programming basics.	8
3	Chapter 3: Computer Arithmetic 1. Number representation (binary, signed, floating-point).	3

	2. Arithmetic operations (addition, subtraction, multiplication, division). 3. ALU (Arithmetic Logic Unit) design. 4. Floating-point arithmetic	
4	Chapter 4: Mono-Cycle Processor Design 1. Overview of single-cycle processor design. 2. Implementation of control and data paths. 3. Single-cycle execution of MIPS instructions.	3
5	Chapter 5: Design of a Multi-Cycle Processor 1. Multi-cycle instruction execution. 2. Control unit design for multi-cycle processors. 3. Comparison of single cycle vs. multi-cycle execution. 4. Performance and cost trade-offs.	5
6	Chapter 6: Pipeline Concept 1. Introduction to pipelining and instruction-level parallelism. 2. Pipeline hazards (structural, data, control). 3. Techniques for hazard reduction (forwarding, stall detection, branch prediction). 4. Performance analysis of pipelined processors.	5
7	**Tutorial**	
	Tut1 : Micro processor architecture	15
	Tut2 : MIPS processor	
	Tut3: Mono-cycle processor and multi-cycle processor.	
	Tut3: Pipeline	
Total		45

D. Teaching and Assessment

1. Alignment of Course Learning Outcomes with Teaching Strategies and Assessment Methods

Code	Course Learning Outcomes	Teaching Strategies	Assessment Methods
1.0	**Knowledge and Understanding**		
K.1	✓ Explain the fundamental principles of processor architecture, including instruction set design and arithmetic operations.	- Lecturing	- Assignments, Quizzes, Exams,
2.0	**Skills**		
S.2	✓ Design and implement single-cycle and multi-cycle processor architectures using simulation tools.	Lecturing Class discussions	- Assignments, , Exams,
3.0	**Values**		

Code	Course Learning Outcomes	Teaching Strategies	Assessment Methods
V.3	✓ Analyze the impact of pipelining on CPU performance and solve pipeline hazards.	- Lectures - Class discussions - Assignments - projects	- Assignments, Report, Quizzes, Exams

2. Assessment Tasks for Students

#	Assessment task*	Week Due	Percentage of Total Assessment Score
1	Practical Work (written or oral)	Weekly	00%
2	Quizzes, Homework assignments	Random	00%
3	First mid Term	8	35%
4	Final Exam	16	65%

E. Student Academic Counseling and Support

Arrangements for availability of faculty and teaching staff for individual student consultations and academic advice:

- Office hours
- Blackboard interface
- Academic advisor
- Bibliotic

F. Learning Resources and Facilities

1. Learning Resources

Required Textbooks	1. **Andrew S. Tanenbaum & Todd Austin.** *Structured Computer Organization.* 6th Edition, Pearson, 2012. 2. **Charles E. Leiserson & James S. Pierre.** *Computer System Design: System-on-Chip & Multicore Architectures.* 1st Edition, MIT Press, 2015. 3. **David A. Patterson & John L. Hennessy.** *Computer Organization and Design: The Hardware/Software Interface.* 6th Edition, Morgan Kaufmann, 2020.
Essential References Materials	- Architecture lessons from Peter Niebert: http://www.cmi.univ-mrs.fr/~niebert/archi2012.php - Introduction au MIPS : http://logos.cs.uic.edu/366/notes/mips%20quick%20tutorial.htm - Introduction to MIPS: http://logos.cs.uic.edu/366/notes/mips%20quick%20tutorial.htm - Table de référence du MIPS : https://pageperso.lis-lab.fr/~alexis.nasr/Ens/Compilation/mipsref.pdf

Electronic Materials	- RISC-V & MIPS Assembly Programming Guide - MIT OpenCourseWare – Computer System Design
Other Learning Materials	- NA

2. **Facilities Required**

Item	Resources
Accommodation	**Classroom board** **Computer lab with the necessary software** **Internet access**
Technology Resources	**Data projector**

G. Course Quality Evaluation

Evaluation Areas/Issues	Evaluators	Evaluation Methods
Effectiveness of teaching and assessment.	Students, course coordinator, Alumni, Employers	Direct/Indirect
Extent of achievement of course learning outcomes.	Faculty, Program Leaders, quality department	Direct
Quality of Learning resources	Faculty, Program Leaders,	Direct, Indirect
Teaching and learning quality and effectiveness.	Students, Faculty Program Leaders,	Direct, Indirect

H. Specification Approval Data

Council / Committee	Computer Engineering Council
Date	11/09/2023